Co-packaged optical and memory chips

Overview

Co-Packaged Optics (CPO) is emerging as the semiconductor industry's answer to this bandwidth bottleneck. By integrating optical components directly with compute or switch chips, CPO promises higher bandwidth, lower latency, and dramatically improved energy efficiency. Advanced packaging technologies, such as 3D chiplets hetero-integration and co-packaged optics (CPO), have become crucial for further improving system performance. Currently, most solutions rely on silicon-based technologies, which alleviate some challenges but still face issues such as warpage. As AI clusters push beyond 100 Tb/s per node, the gap between what silicon can generate and what traditional copper interconnects can deliver is widening fast. Three hurdles are now colliding: First, power delivery is nearing practical limits. Adding GPUs no longer scales linearly, with power and. As datacenters strive to meet escalating demands for efficiency and bandwidth, particularly with the integration of AI and ML technologies, optics is poised to play a crucial role in shaping the future of interconnect architecture and performance. This technology can immediately boost today's AI/ML compute power to train larger neural networks that can perform more complex tasks. Now, imagine that some of the most essential roads are congested.

Article Content

Aug 12, 2025

Yole Group

Yole Group - Access daily business, market & technology updates in the semiconductor industry, our Analysts'' Analysis and Presentations and more

Sep 03, 2025

Five Key Trends of Co-Packaged Optics (CPO) in 2026

These pressures are driving renewed momentum behind co-packaged optics (CPO). According to LightCounting, sales of lasers and photonic integrated

Nov 06, 2025

Intel shows OCI optical I/O chiplet co-packaged with

Explosive AI infrastructure growth is bringing high bandwidth density and low power performance requirements to compute architectures which optical

Apr 03, 2026

NVIDIA Vera Rubin NVL72: Full Specs & Platform

NVIDIA announced its most ambitious AI platform yet at GTC 2026. Here''s the full spec breakdown on every chip, rack, and configuration.

May 04, 2026

Molex Announces Agreement to Acquire Teramount Ltd. | Molex

Molex announces agreement to acquire Teramount, adding TeraVERSE detachable, passive-alignment fiber-to-chip technology to accelerate scalable co-packaged optics for AI, cloud

Feb 10, 2026

Co Packaged Optics (CPO) – Scaling with Light for the

Co-Packaged Optics (CPO) has long promised to transform datacenter connectivity, but it has taken a long time for the technology to come to market,

Apr 08, 2026

Marvell Announces Breakthrough Co-Packaged Optics

Marvell Announces Breakthrough Co-Packaged Optics Architecture for Custom AI Accelerators SANTA CLARA, Calif. — January 6, 2025 — Marvell

Dec 16, 2025

LIVE WEBINAR | CO-PACKAGED OPTICS: POWERING THE NEXT

Powering co-packaged optics with advanced semiconductor equipment and process innovation. April 28 – 8 am SGT (Singapore, 04/28) – 5 pm PST (San Francisco, 04/27) The webinar has now ended.

Apr 05, 2026

TSMC''s “Three-Layer Cake” Theory: Why Optical Interconnects Are

Key Points TSMC introduced a “three-layer cake” theory for AI chip architecture, emphasizing Compute, Heterogeneous Integration & 3D IC, and most importantly, Photonics and

May 03, 2026

$LPK $LPKFF Part One of the Re-Rate is Complete. Part Two Takes

This technology is essential for next-generation AI chips. Organic substrates are at their physical limit. Glass is the answer for 1.6T-class signaling, high-bandwidth memory (HBM)

Nov 09, 2025

The Third Time Will Be The Charm For Broadcom

If Broadcom says that co-packaged optics is ready for prime time and can compete with other ways of linking switch ASICs to fiber optic cables, then it

Nov 10, 2025

Next generation Co-Packaged Optics Technology to Train & Run

A co-packaged optic module design was developed to support electronic and optics compatibility, industry standards where applicable and scaling for design, process, assembly, test, pluggable

Apr 10, 2026

Understanding Co-Packaged Optics: The Need for

Discover how Co-Packaged Optics (CPO) integrates photonics and chiplets to overcome bandwidth bottlenecks and power challenges in modern computing.

Mar 31, 2026

Co-packaged Optics: all eyes on high-performance

Disaggregated design distinguishes the compute, memory, and storage components found on a server card and pools them separately. Using advanced in-package

Nov 21, 2025

Co-packaged Optics Market 2026-2034 Analysis:

Co-packaged Optics Market Company Market Share This comprehensive report, spanning a Historical Period of 2019-2024 and a Forecast Period of 2025-2033,

Oct 10, 2025

Next Up for Custom AI Accelerators: Co-Packaged Optics

With AI, it''s finally happening. Marvell earlier this month announced that it will integrate co-packaged optics (CPO) technology into custom AI

Aug 25, 2025

Predicting Cost Trends for Widespread Co-Packaged Optics Adoption

Co-packaged optics technology faces significant cost structure challenges that currently limit its widespread adoption across data center and telecommunications markets. The primary cost

Mar 15, 2026

SMoazeni_UW

From a system-level perspective, this technology brings in new possibilities including adding memory access and compute functionalities to utilize co-packaged optics as a “co-processor”.

Jan 26, 2026

Optics Primer, Part 3: Co-Packaged Optics (CPO)

Optics Primer, Part 3: Co-Packaged Optics (CPO) From EML lasers and DSPs to silicon photonics and external CW lasers. How CPO works and the

Sep 30, 2025

Co-packaged Optics: The Next-Gen Data Center Tech

This application will guide you in understanding this groundbreaking technology that tightly integrates optics with chips, and explore how it addresses

Dec 09, 2025

AMD Acquires Enosemi to Accelerate Co-Packaged

Co-packaged optics can deliver higher bandwidth density and better power efficiency than traditional approaches, representing a transformative step

Dec 16, 2025

Co-packaged optics (CPO): status, challenges, and

Co-packaged Optics (CPO) is an advanced packaging technology

Nov 30, 2025

RANOVUS delivers industry''s first 6.4Tbps Co

Ranovus'' standards compliant Odin® direct-drive CPO 3.0 optical interconnect, with 4pJ/bit energy efficiency, including the laser, delivers the

Aug 15, 2025

Co-Packaged Optics – List of Examples – Ansys Optics

Ansys Lumerical and Zemax toolsets provide the best-in-class solutions to simulate and design complete optical coupling systems for co-packaged optics and other integrated photonics applications.

Dec 22, 2025

Nvidia updates data center product roadmap following LPU launch at

According to the chip designer, the Feynman GPU will incorporate die stacking and custom high-bandwidth memory to help scale performance and increase memory bandwidth.

Jul 18, 2025

FormFactor Targets Revenue Doubling by 2030 on AI Chip Testing

FormFactor said it aims to double revenue to $1.6 billion by 2030 and more than double non-GAAP EPS, driven by growth in high-performance computing, advanced packaging, HBM and

Mar 08, 2026

Electronic Chip Package and Co-Packaged Optics (CPO) Technology

With the growing demand for high-performance computing (HPC), artificial intelligence (AI), and data communication and storage, new chip technologies have emerged, following Moore''s Law,

Oct 04, 2025

Co-packaged optics: The future of data centers

Discover how co-packaged optics (CPO) is revolutionizing hyperscale data centers. Learn how Corning''s cutting-edge technology boosts AI

May 20, 2026

Co-Packaged Optics — a deep dive | APNIC Blog

These high-density edge-mounted optical engines directly interface with the core die through short, chip-to-chip connections through the organic

Jun 01, 2026

Co-packaged Optics Boost AI Hardware Efficiency

Co-packaged optics are becoming more relevant for AI hardware. The idea is simple: instead of sending data through longer electrical paths to separate optical transceiver modules (modules that ...

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